

Design and Evaluation of a Low-Level RF Control System Analog/Digital Receiver for the ILC Main LINACs

Keywords: ILC Main LINACs, LLRF, Digital Receiver, Vector Sum, high frequency electronics design

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Abstract: The proposed RF distribution scheme for the two 15 km long ILC LINACs, uses one klystron to feed 26 superconducting RF cavities operating at 1.3 GHz. For a precise control of the vector sum of the signals coming from the SC cavities, the control system needs a high performance, low cost, reliable and modular multichannel receiver. At Fermilab we developed a 96 channel, 1.3 GHz analog/digital receiver for the ILC LINAC LLRF control system. In the paper we present a balanced design approach to the specifications of each receiver section, the design choices made to fulfill the goals and a description of the prototyped system. The design is tested by measuring standard performance parameters, such as noise figure, linearity and temperature sensitivity. Measurements show that the design meets the specifications and it is comparable to other similar systems developed at other laboratories, in terms of performance.

1. Introduction

The proposed international linear collider (ILC) will be an electron/positron collider operating at 500 GeV (possible upgrade to 1 TeV) and it will be composed of two damping rings, electron/positron source, detectors and two LINACs. The study in this paper applies also to other ILC-style LINACs, where one klystron drives multiple superconducting (SC) cavities. As presented in the reference design report for the ILC (RDR) [1], the RF distribution for the LINACs foresees 560 RF units, each of them composed of one klystron driving 26 SC cavities. The low power section of the RF system, also denoted as the low-level RF (LLRF), takes care of the control of the vector sum of signals coming from the SC cavities. The LLRF stabilizes the amplitude and phase of the vector sum at the desired set point by means of feedback and feedforward regulation techniques. In order to calculate the correction that is applied to the klystron, the LLRF control uses 96 RF signals coming from one RF station (26 cavities). As a result, for the two LINACs, the overall sum of the RF signals that are processed by the multichannel receiver system equals 50 000. The high channel count has a major impact on the design of the LLRF receiver section, where all the incoming signals need to be downconverted and digitized. The process of downconversion and digitalization suffers from noise, nonlinearities, and temperature dependent processes. In this paper we present the design strategies to address these problems and we exploit these strategies to implement a possible solution for the multichannel analog/digital receiver for an ILC style LINAC LLRF control system.

2. Requirements

The two main parameters that have the biggest impact on the design of the receiver are the performance and the high number of channels. In the RDR, the performance requirements are given in terms of controlled amplitude and phase of the RF fields and they are derived from the requirements for luminosity of the collider. These numbers equal to 0.5 % and 0.24° for correlated errors (e.g. ground motion, reference line drifts, beam loading, etc.) and 1.6 % and 0.48° for uncorrelated errors (e.g. noise in one channel of the receiver). The errors are partitioned among the reference system (drifts of the reference line between RF stations), the perturbation sources of the cavity (microphonics, Lorentz force detuning and beam loading) and the LLRF electronics. The error from the LLRF electronics is mainly defined by the errors from the receiver and the error from the LO generation/distribution [2, 3]. The uncorrelated error introduced by one channel of the receiver (with the LO generation and distribution) that we aim for must be at least 20 times lower than the overall uncorrelated errors given in the RDR. This equals to 0.08 % RMS and 0.024° RMS for amplitude and phase respectively. Other disturbances like harmonics generated by the nonlinear electronics, coupling among adjacent channels and temperature dependent drifts also have considerable effects on the system performance. However, they are not explicitly given in the RDR. In order to define some values for these parameters, as our design goals, we followed the philosophy that they must be limited by the most expensive part in the receiver chain, which is the analog-to-digital converter (ADC). We therefore aim for an isolation among channels that is higher than 90 dB and the second and third harmonics generated by the receiver must

not exceed -75 dBc. Furthermore we demand that the change of amplitude and phase over large temperature swings (15 °C) meets uncorrelated amplitude and phase error values given above. We also expect that the resolution of the ADC will define the uncorrelated noise spectral density (NSD) of the receiver system at the output.

In addition to performance, the design has to account for the high number of RF channels that need to be processed. Due to the higher probability of failure, the high number of channels calls for a robust design to fit mean time between failure (MTBF) requirements and a modular design to minimize the mean time to repair (MTTR). In order to minimize MTBF we need to minimize the number of components in the system, which also means we aim for a simpler and lower cost design. Modularity can be achieved by properly grouping processing sections of the system which will eventually result in a more versatile design, with the possibility to be reused on other RF systems. The system with high number of channels also demands a high degree of automation, which would otherwise be impossible to calibrate, reprogram or diagnose in a short time period. Finally, the high channel count requires a cost and power sensitive design. The power consumption of the LLRF electronics that we aim for is less than 200 W per one RF station (96 channels).

3. System Design Strategy

The first step towards meeting the requirements for good performance, versatility and ease of automation is achieved by choosing the digital approach to system design. The commonly adopted digital architecture used in modern LLRF systems [4, 5] is based

on the software defined radio (SDR) design, developed for the telecommunication market. The SDR philosophy is to digitize the signal as close to the antenna (cavity pick-up probe) as possible. This reduces the number of components, simplifies calibration of multiple channels and increases flexibility in digital signal processing. The typical SDR architecture uses direct sampling of RF signals with no downconversion to intermediate frequencies (IF). However, direct sampling degrades the signal-to-noise (SNR) ratio of the system due to the clock and aperture jitter of the ADC and digital-to-analog converter (DAC). For this reason we chose instead to use the heterodyne approach, where the input RF signal at 1.3 GHz is downconverted to an IF at 13 MHz and then digitized.

The other important decision that has a major impact on modularity and cost is to use high channel density boards. This minimizes the number of boards needed per one RF station, decreases the group delay, simplifies the interconnections between the boards and reduces the possibility of failure. However, this decision also increases the number of traces and parts on the printed circuit board (PCB) close to the ADC. This eventually degrades signal integrity and makes the layout more complex. An additional problem associated with the high number of channels is finding an RF connector with satisfying isolation between channels that is compact and has acceptable return loss at 1.3 GHz. Many of the high density and compact connectors we tested, showed very poor isolation (> -50 dB) and return loss performances (> -15 dB) at 1.3 GHz. For this reason we decided to split the analog and the digital processing into two boards (see Fig. 1) and use the eight channel coaxial connector (Harting, mini-coax) to interconnect the two boards.

Figure 1. The two printed circuit boards are the eight channel analog receiver board [6] (on the left) and the 33 channel digital board [7] (on the right) also referred as the multichannel field controller module (MFC).

3.1 Digital Board Design

In order to implement a high channel density board and at the same time solve the problem with the layout and signal integrity, extensive research has been done on various types of ADCs that the market is offering. The octal ADC (Analog Devices Inc., AD9222) with serial low voltage differential signal (LVDS) output lines is a very convenient solution to this problem. It integrates 8 channels on one chip and it has only two (differential pair) output lines per ADC channel.

As mentioned in the introduction, we expect the NSD at the output of the receiver system to be equal to the NSD of the ADC, which was measured to be -147 dBc/Hz. Even though this noise level already satisfies the requirements for uncorrelated amplitude and phase errors given in the introduction, the expectations are even more optimistic. If we assume that the noise is uncorrelated, the vector sum will improve the SNR at the output of the ADC by app. 14 dB. It is worth noting that the relatively high ADC aperture jitter (800 fs) has little effect on the output NSD when the IF frequency is less than 50 MHz. For an IF of 13 MHz, the noise spectral density (NSD, normalized to the carrier power) due to the aperture jitter equals -160 dBc/Hz, which is calculated using equations given by Kobayashi [8].

The eight channels ADC allows for a compact design and it turns the limitation in the maximum number of channels per board over to the front panel space available for

the mini-coax connectors. The VXI form factor can accept no more than five, eight channel mini-coax connectors that feed 33 ADC channels and four DAC channels. Thus, three digital boards cover the requirements for one RF station. Fig. 1 (on the right) shows the implementation of the digital board.

3.2. Analog Board Design

For the same reasons as in the case of the digital board, we investigate the idea of using multiple high channel density boards for the analog board design. The number of RF channels per analog board is again defined by the size of the input RF connector. Using the N-type RF connector in the front of the board, allows connection of the rigid cables that come from the cavities directly to the analog board. Consequently, there is no need for extra cables, extensions, patch-panels or feed-throughs. We managed to put nine N-type connectors on a 9U (40 cm) board, eight for the receiver and one for the transmitter. This means we need 12 analog boards along with three digital boards per one RF station (96 RF channels).

Although the bulk of the analog receiver is a rather simple frequency translator, the receiver needs to be optimized for noise performance, coupling between channels, linearity and temperature sensitivity. The requirements for these parameters are given in the introduction section. The two main issues that proved to have the greatest impact on the performance of the analog board are the choice of the mixer and the topology of the LO distribution.

The Mixer: The mixer parameters that affect the presented design the most are the mixer linearity, the RF to LO isolation and the input impedance at the mixer ports. Extensive measurements of these parameters for various mixers helped us to choose the most appropriate mixer for this design. These measurements are presented in more detail in literature [9]. The SYM-25DLHW (Mini Circuits) level 10 (+10dBm LO power) mixer represents a fair compromise between good linearity and low LO to RF coupling. Measurements also show that using LO amplifiers directly on the LO port increases coupling between channels and the close-in phase noise of the downconverted signals. For this reason, active mixers with embedded LO amplifiers are not a good choice for this application. Coupling between RF channels depends mostly on the RF to LO isolation. The RF signal couples on the LO port and propagates through the LO distribution. By mixing with the LO, it translates on the IF port of the adjacent channels as shown in Fig. 2 (thick solid arrow). This problem can be solved by properly matching the mixer ports and by choosing the most suitable architecture for the LO distribution (see next section). The implementation of the IF port matching is shown in Fig. 2. This helped to reduce the coupling between adjacent RF channels to app. -70 dB. The remainder of the coupling is caused by the transmission lines that connect the IF circuitry and the output mini-coax IF connector. Burying these lines between two ground planes (stripline) helped reducing the coupling to less than -80 dB. Standard coupling reduction design techniques, like proper shielding of each high frequency section and channelization of ground and power planes, have also been used.

LO Distribution: The other design issue concerning the analog receiver is the topology of the LO distribution. The problem is that the LO signal at 1.313 GHz and with

+ 20dBm input power must be split and distributed to 9 points over 15 cm long traces on RO4530 (Rogers Corporation) circuit board material. Since the power at each of these 9 points must be at least +10 dBm, additional amplification is needed. We discard the 8 amplifiers option, where each LO port has its own amplifier, for the reasons mentioned in the previous paragraph. Using two amplifiers that are placed in between three 1:4 power splitters (see Fig. 2 LO distribution module), turns out to have several advantages over the single input amplifier option. The main advantages are good matching, low coupling between RF channels, compactness, low power dissipation, low cost and no need for high power amplifiers.

4. Implementation of the Receiver System

Fig. 2 shows the test setup that helped us to evaluate the proposed multichannel analog/digital receiver. It is composed of the LO generation/distribution, the analog receiver and the digitizer (digital receiver). The analog receiver comprises eight equal channels that accept eight pulsed (1.3 ms pulses with 5 Hz repetition rate) RF (1.3 GHz) signals coming from the cavities. For the measurements presented in this paper, the eight RF signals are generated by the dielectric resonator (DRO, Poseidon Scientific Instruments) and split into eight equal RF channels. In the analog receiver, the RF (1.3 GHz) signals are downconverted to the IF at 13 MHz by mixing with the LO at 1.313 GHz. Sampling of the IF signal is carried out on the digital board. From the ADC, the LVDS lines transfer the data to the Cyclone II (Altera) field programmable gate array (FPGA). On the FPGA we implemented a digital downconverter that generates the in-

phase (I) and quadrature (Q) baseband components of the acquired data. Data is then filtered and decimated by using the Hogenauer [10] realization of the cascaded integrator-comb (CIC) filter. In real operating conditions there will be up to 96 RF signals coming into 12 analog receiver boards. The 26 digitized signals will be coherently summed (vector sum) on the digital board before applying the correction to the klystron. Fig. 1 shows the practical implementation of the receiver presented in Fig. 2.

Figure 2. The test setup/schematic of the one channel receiver system and LO generation/ distribution used for the evaluation. The IF (13 MHz) signal is sampled by the digital board (MFC) and downconverted to baseband. For the multichannel system we have as many analog and digital receiver sections as there are channels. The thick solid arrow close to the mixer in the analog receiver module shows the coupling path between two channels.

5. Results

We evaluated the presented design by measuring standard parameters like noise, linearity, coupling and temperature sensitivity.

5.1. Noise Characterization

Among all the different modules that compose the LLRF control system, the receiver is the most critical in terms of noise contribution. According to basic control theory, the transfer function between the disturbances added in the receiver and the output of the cavity equals one (for high loop gains). Other disturbances in the feedback

loop, e.g. from the transmitter, also perturb the cavity output. However, these influences are reduced by the loop gain and they are neglected in this paper.

Analog Board: Using equations from Pozar [11] and datasheet data for gains, attenuations and noise figures shown in Fig. 2, you can calculate the equivalent noise figure of the analog receiver, which equals 29 dB. The noise figure is mainly defined by the attenuation before the operational amplifier shown in Fig. 2. The theoretical NSD at the output of the analog receiver equals -155 dBc/Hz, which is very close to what was measured by using a spectrum analyzer. As presented in literature, [12] noise figures from datasheets show only broadband noise (amplitude noise) performance of devices and no assumption on close-in (phase noise) can be made based on this data. We therefore measured phase noise performances of the analog board. Fig. 3 shows the single-side band spectrum of the analog receiver's uncorrelated residual phase noise. The integrated RMS phase jitter of the blue spectrum presented in Fig.3 equals to 0.00018°. Details about residual phase noise measurements techniques are given in [13]. In our case we mixed two adjacent 13 MHz outputs from the analog receiver in quadrature and obtained the spectra shown in Fig. 3. It is hard to draw any conclusions from Fig. 3 about residual phase noise profile below 1 kHz since the AM noise on the RF and LO ports of the mixer (green line) dominates. The AM noise (green line) is lower than the broadband NSD calculated using the noise figure method because the mixer was driven in saturation.

Figure 3. Measurements of uncorrelated residual phase noise of the analog receiver. LO amplifiers on the LO port (red trace) give worse phase noise performances than the amplifiers placed as shown in the LO distribution (blue trace) module in Fig. 2.

Digital Board: The modeled noise added by the digitizer has a uniform distribution and the SNR given in the datasheet equals 70.4 dB over one Nyquist zone. When normalized to 1 Hz the NSD of the AD9222 is -147dBc/Hz. The aperture jitter contribution is neglected for the reason given in the system design strategy section. We also neglect the amplitude noise contribution from the analog board since the NSD is lower than the NSD of the digital board as shown in the previous paragraph. The measured NSD at the output of the processing chain (test point 1 in Fig. 2) is shown in Fig. 4. The bandwidth is reduced to app. 100 Hz - 100 kHz (303 times) due to the decimation process in the FPGA. As shown in Fig. 4, the close-in phase noise has spurs close to 1 kHz that are produced by the LO generation/distribution section. They were not measured in Fig. 3 because the residual phase noise measurement, adopted for this measurement, cancels out all coherent disturbances. The integrated RMS amplitude and phase uncertainties for the spectra shown in Fig. 4 are 0.0022% and 0.0044° RMS from 100 Hz to 100 kHz. However, these values are expected to be smaller due to the process gain of the vector sum of 26 channels per RF station. Fig. 5 shows the spectrum of the acquired data before the vector sum (red line) of eight RF channels and after the vector sum (blue line). The process gain is app. 9dB.

Figure 4. Amplitude and phase noise detected at the output of the receiver system. The FFT resolution is app. 13 Hz and the number of samples is 16k. The sampling frequency at the ADC is 62.524 MHz (1313/21 MHz). The decimation in the CIC is 303. The main discrepancies between the simulated data (red trace) and measured data (blue trace) are caused by spurs from the LO generation/distribution.

Figure 5. FFT of 32k samples for one channel (red spectrum) and for the vector sum of eight channels (blue spectrum). The input IF frequency is 13 MHz and the sampling frequency is 62.525 MHz.

5.2. Coupling between channels

Coupling between channels is undesirable since it represents additional feedback paths that might cause instabilities in the main feedback loop. The measured coupling on the digital board is less than - 90dB. The coupling path on the analog board is shown in Fig.2 with a thick solid arrow inside the analog receiver module. Table 1 shows measurements of coupling between any pair of channels at test point 1 (see Fig. 2).

Table 1. Channel-to-channel coupling matrix between 8 channels measured at the end of the receiver shown in Fig. 2 (test point 1). All the values are in dB. The highest coupling was measured between channels that are closer together.

5.3. Temperature Sensitivity

To characterize the performance of the analog board as a function of temperature, we put the board shown in Fig. 2 (on the left) in a temperature regulated chamber. The measurements of phase and amplitude were performed by using the same system as the one shown in Fig.1. The temperature inside the chamber varied from 30°C to 50°C, which dominated drifts of the circuitry and cables outside the temperature chamber. The measured temperature sensitivity as a function of temperature change of the analog board

is shown in Fig. 6. Temperature sensitivity of the receiver equals to app. 0.5 °/°C for phase and 0.1 %/ °C for amplitude.

Figure 6. Phase and gain sensitivity as a function of temperature in the chamber. The fluctuation of each individual measured value is 0.01% RMS.

5.4. Linearity

Each individual cavity probe RF signals is calibrated in both magnitude and phase in the FPGA. These calibrated signals are then added to provide a vector sum that equals the total field seen by the electron bunches passing through the cavities. Nonlinearities in the downconverter chain will cause errors in the vector sum if cavity gradients deviate from the operating point of the calibration. Nonlinearities may also cause transformation from amplitude modulation to phase modulation and vice versa. Linearity was measured indirectly by measuring the power level of the harmonics. Fig. 8 shows the measured power level of the main component (13 MHz), second (26 MHz) and third harmonic (39 MHz) at the output of various sections in the analog receiver. In order not to corrupt the measurements, the output of the receiver was not filtered. In case when the $P_{in} = +10\text{dBm}$ (normal operating point) the second and third harmonic contents at the output of the RF section equals -50dBc and -55dBc respectively. For the IF section these two values equal -65dBc and -55dBc respectively. When measuring the whole receiver (presented as R_c measurement) the harmonics content is higher (-40dBc and -48dBc).

Figure 7. Linearity measurements of the RF section, IF section and analog receiver as a whole (Rc). The solid line are the main components at 13 MHz, the dashed lines are the power levels of the second harmonic (26 MHz) and the dotted lines are the power levels of the third harmonic (39 MHz). Circles show the operating point for the whole receiver. There is no IF filtering used for these measurements.

6. Discussion

Results show that the presented receiver design meets the specifications defined in the system requirements section. Due to a modular, robust, cost effective and high performance design, this receiver is suitable for machines like the ILC main LINACs and the ILC bunch compressor. Detailed measurements show that the component that defines the broadband (more than 2 kHz away from the carrier, see Fig. 4) noise performance is the ADC (see Fig. 4). This agrees with the initial design strategy. We also calculated that the aperture jitter of the ADC can be neglected since its contribution is app. 10 dB lower than the quantization noise level. Fig. 4 shows that at close-in frequencies, less than 2 kHz away from the carrier, the noise is not white and it is defined by the LO generation and distribution modules. The measured spectrum in Fig. 4 agrees within 2 dB with the simulated spectrum. The integrated RMS amplitude and phase uncertainty at test point 1 equals to 0.0022% and 0.0044° in the bandwidth from 100 Hz to 100 kHz. At other laboratories, for instance DESY [3, 5] or LBNL [4], they measured similar noise performances. The measured values for integrated phase jitter from 19.9 Hz to 100 kHz are 0.004° (0.2 ps at 50 MHz) for LBNL (calculated by using data in [4] and using 50 MHz for IF frequency) and 0.003° from 10 kHz to 1 MHz at DESY. The amplitude uncertainty measured at DESY is 0.003% from 10 kHz to 1 MHz.

We believe that the penalty in noise performance of the 12 bit AD9222 is offset by the effective processing gain from summing 26 RF channels. The realization of the high channel count, low power and low cost MFC module was possible mainly because of ADC characteristics. We expect that there will be continued advancement in the performance of the multichannel serial ADCs, e.g. resolution, sampling clock, latency, etc. The presented design allows us to easily take advantage of these chips when they become available, without affecting other design goals.

In addition to noise performance, channel to channel isolation was also thoroughly studied. By using the design strategies described above, the coupling between adjacent channels was greatly reduced ($< -80\text{dB}$). This also proves that splitting the microwave and digital domains was a good choice. It is worth noting that we didn't notice any additional increase in noise or disturbances due to the separation. The main limitation for coupling is still the analog receiver. Additional studies would be necessary to achieve isolation close to -90 dB .

To minimize distortion, the operating point was chosen such that the mixer and the op-amp have minimal nonlinear contributions while still maintaining an overall low noise figure. The amplified harmonics that are generated in the mixer are filtered by the output low-pass filter and the band-stop filter at 26 MHz. Filtering attenuates the second and the third harmonic below -75 dBc . In order to improve linearity, a higher level mixer or an active mixer could be considered. However, as shown above, active mixers are not a good choice from the point of view of noise performances (see Fig. 3) and coupling. Furthermore, a higher level mixer (e.g. level 17 or more) presents a bigger challenge for the low noise LO distribution and coupling of the LO on the PCB board.

Finally, amplitude and phase drifts are likely to be several percent in amplitude and several degrees in phase according to measurements in Fig. 7. A first order correction to thermal drift is to compare the phase of the cavity signal with the phase of the reference signal that has been down-converted and digitized with an adjacent receiver channel. According to Doolittle, [13] this will cancel out the slow changes in phase that are common to all the channels. For a more precise correction, a more complex drift calibration scheme has to be developed. The comparison of all the main measured and expected parameters is given in Table 2.

Table 2. Measured and expected values for performance parameters of the whole receiver.

7. Conclusion

The presented design offers a modular, compact and cost effective solution for LLRF applications that require high channel count receivers. The receiver system comprises the analog and the digital module. To control one ILC-style RF station, three digital boards and 12 analog boards are needed. Although the number of boards, hardware complexity and cost are reduced, the measured performance is comparable to other low channel count receiver systems developed at other laboratories. In the paper we identified the limiting components in terms of performance. This gives a starting point for further system customization and optimization.

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Figure 1
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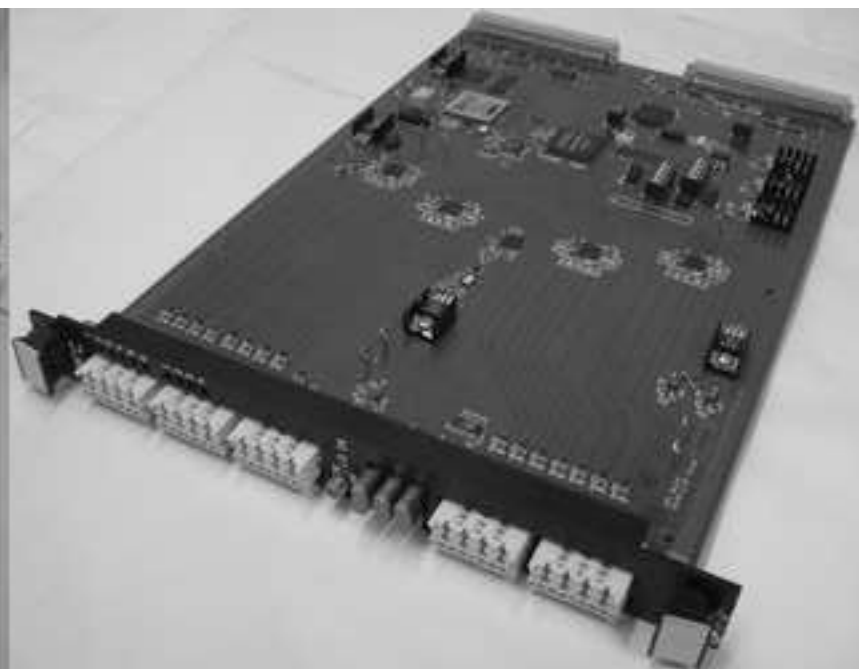
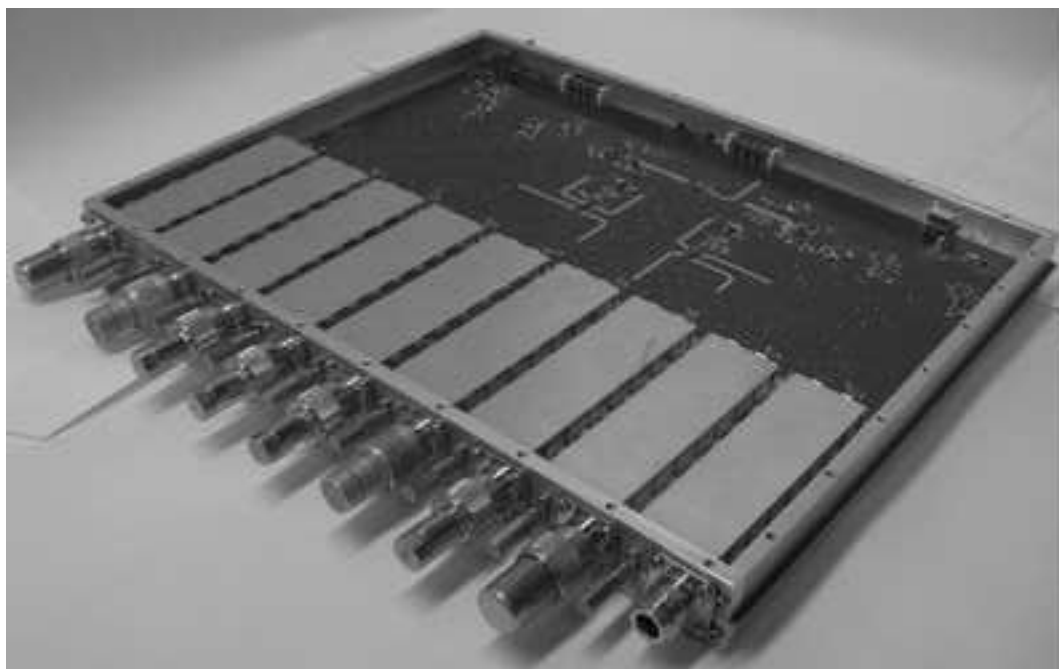


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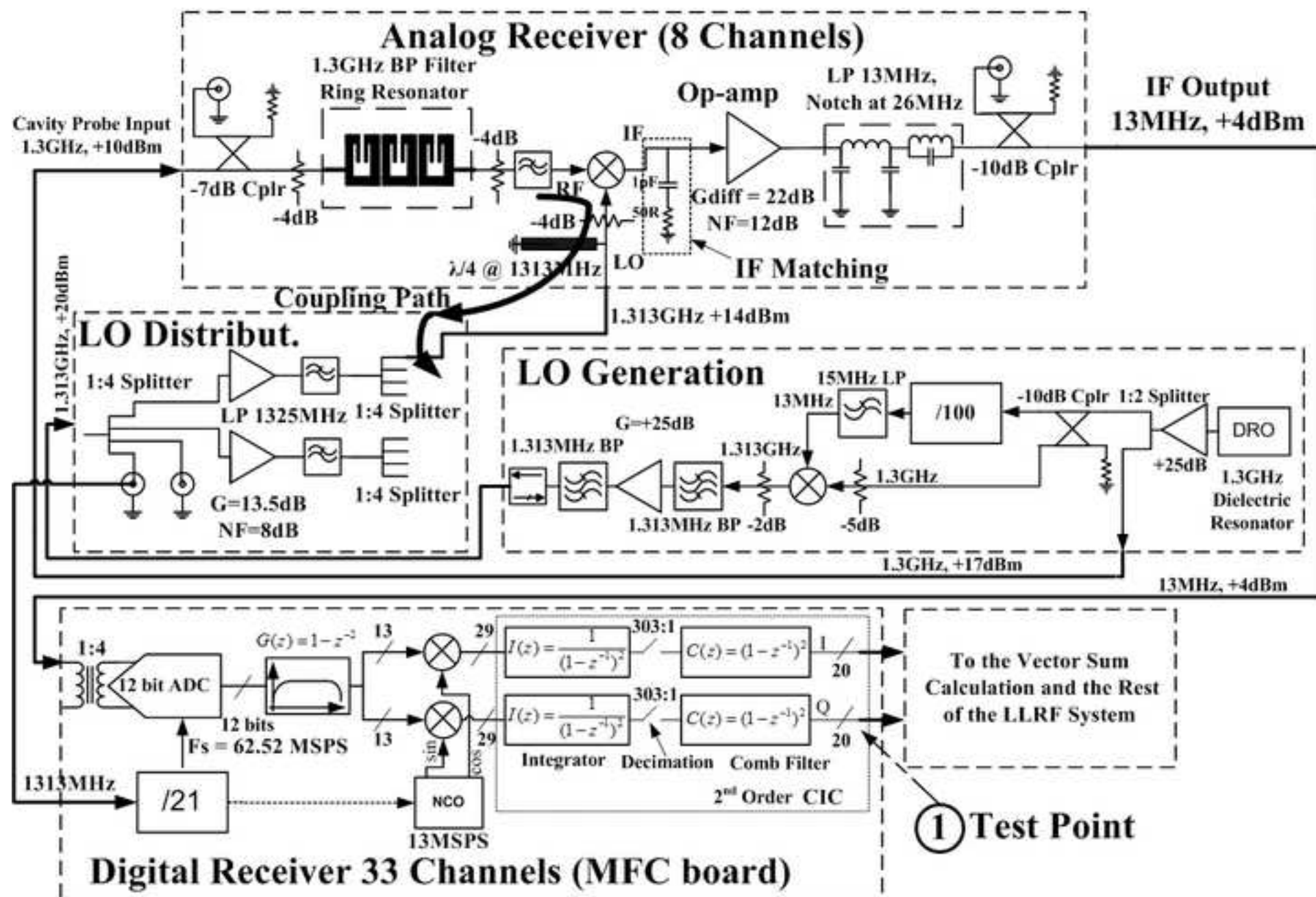


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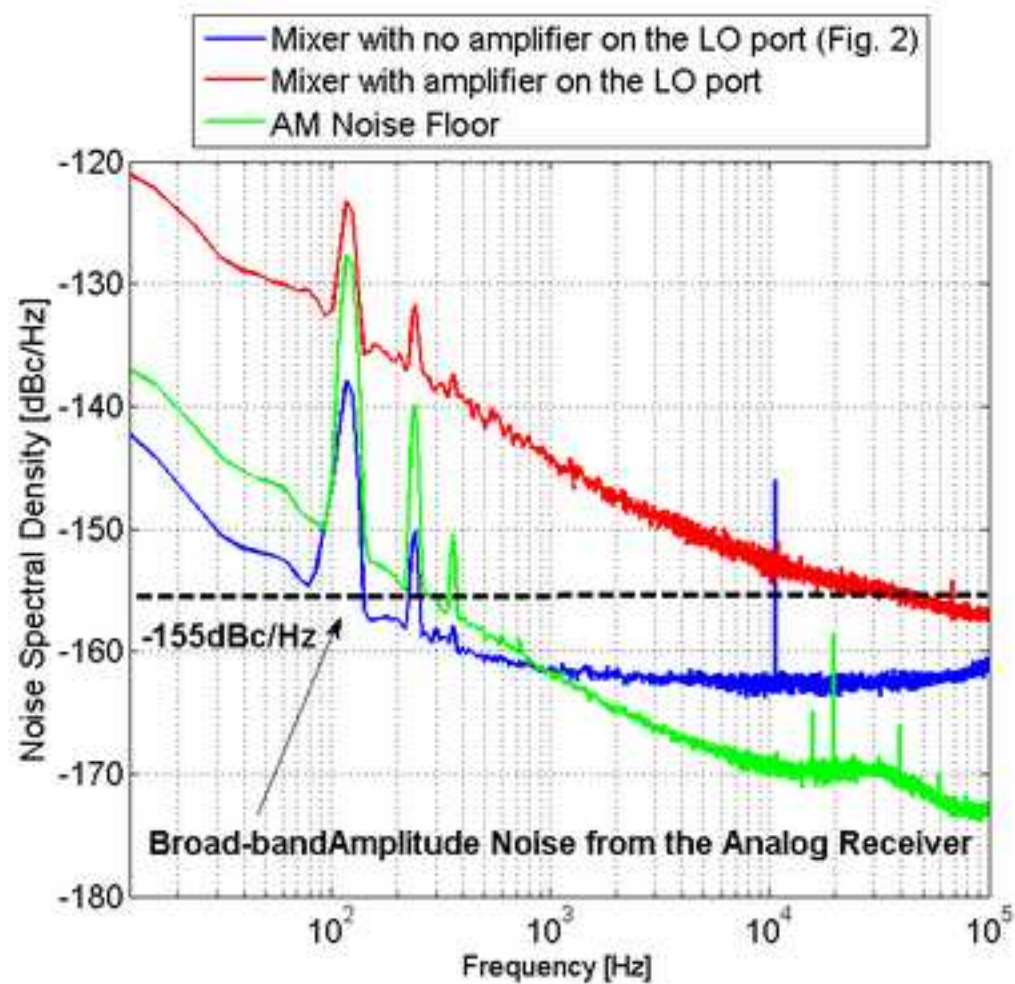


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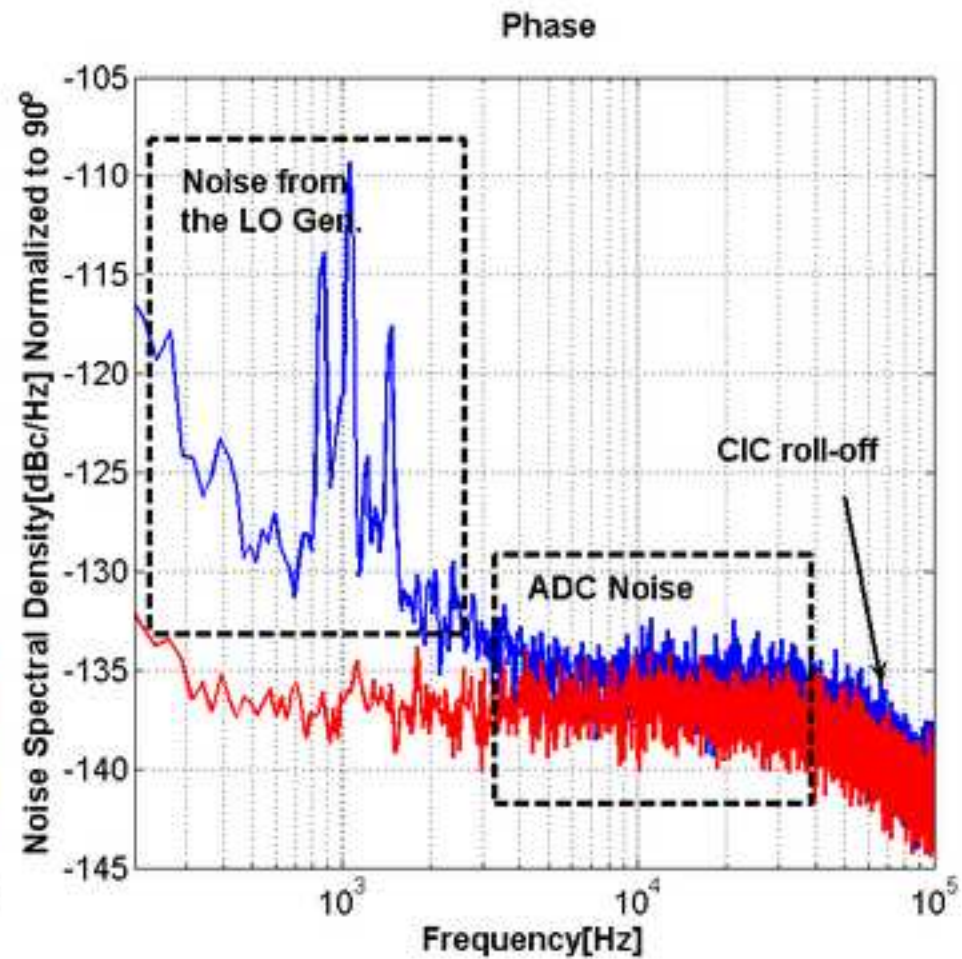
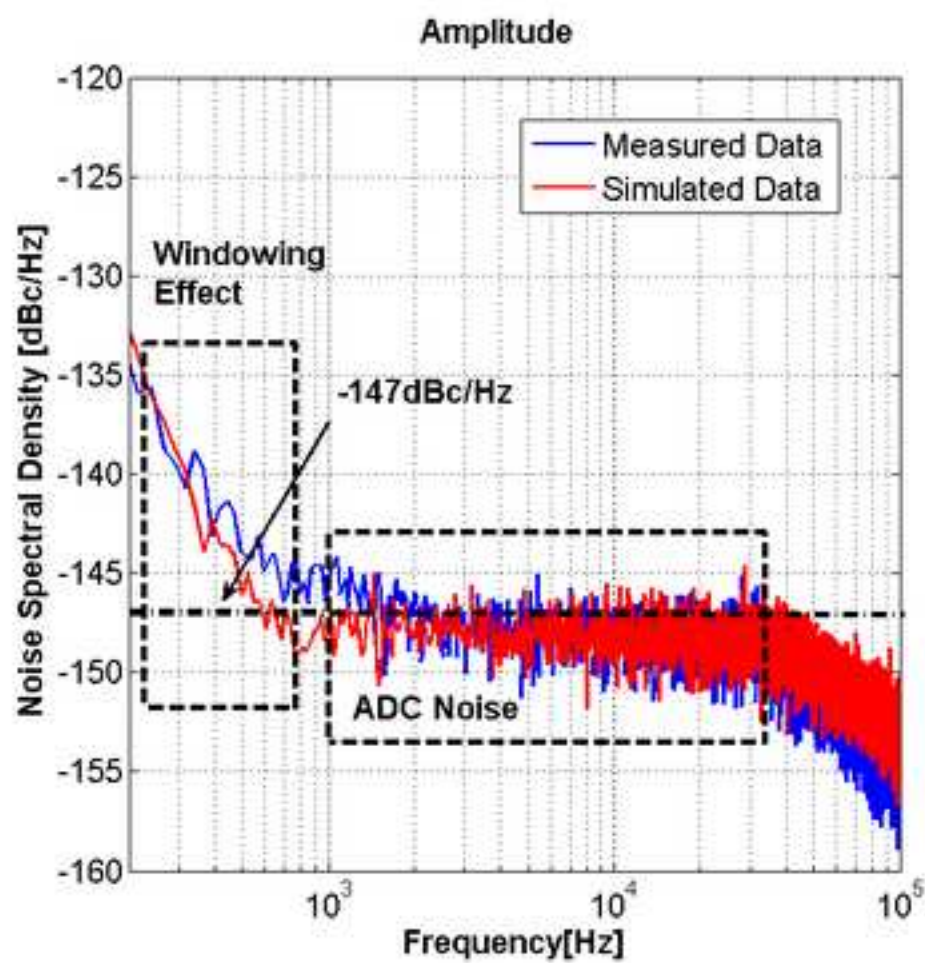


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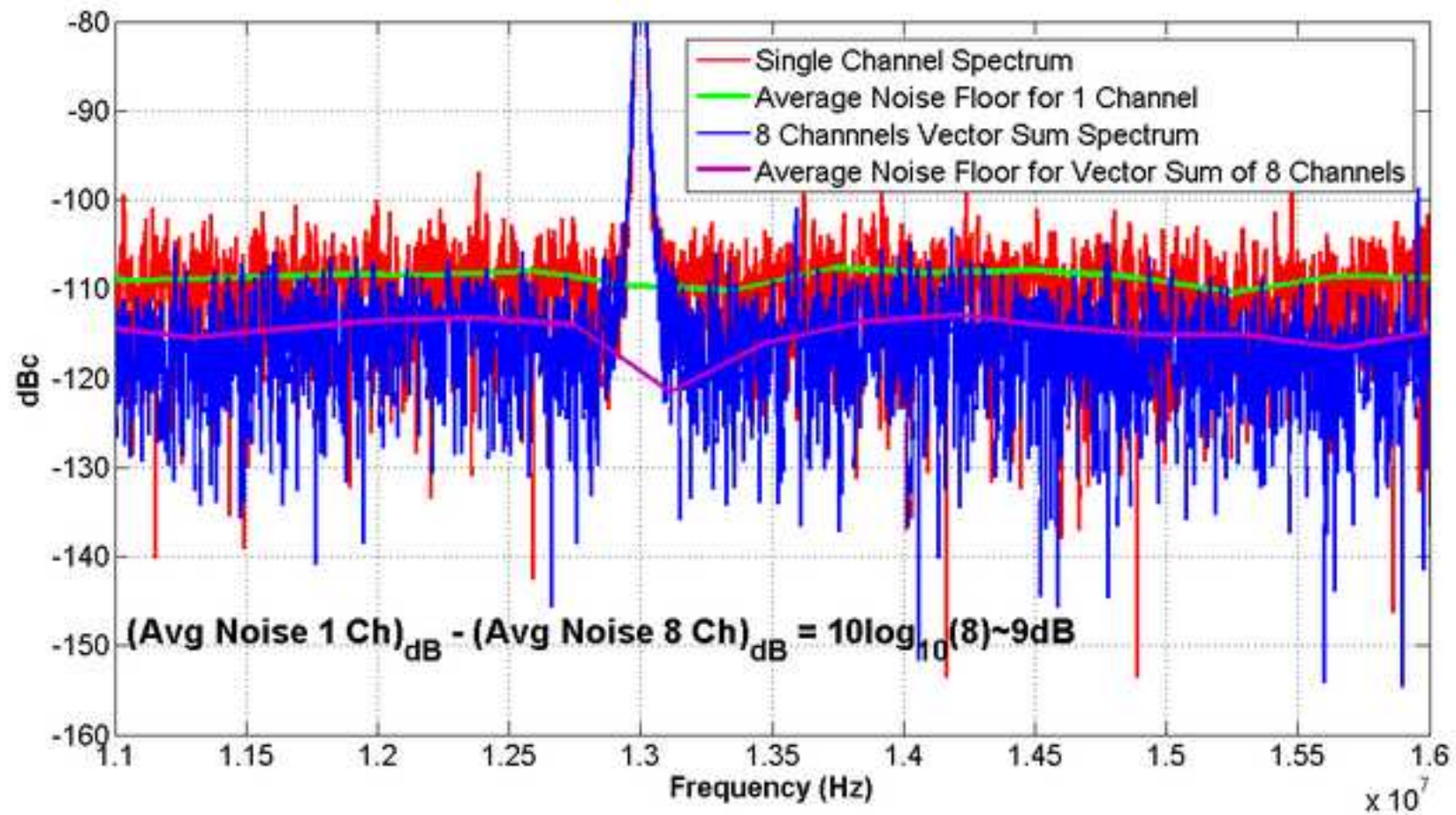


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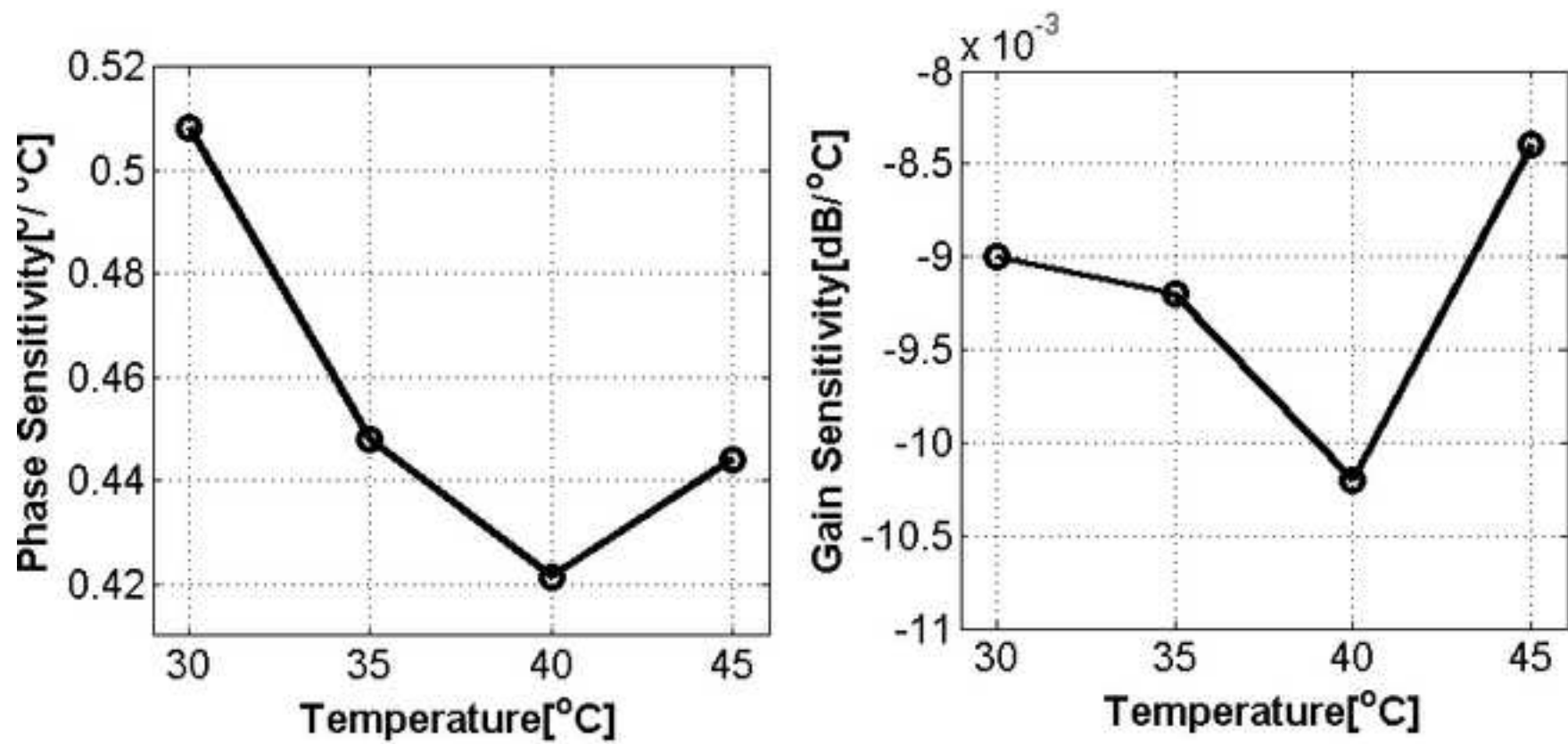


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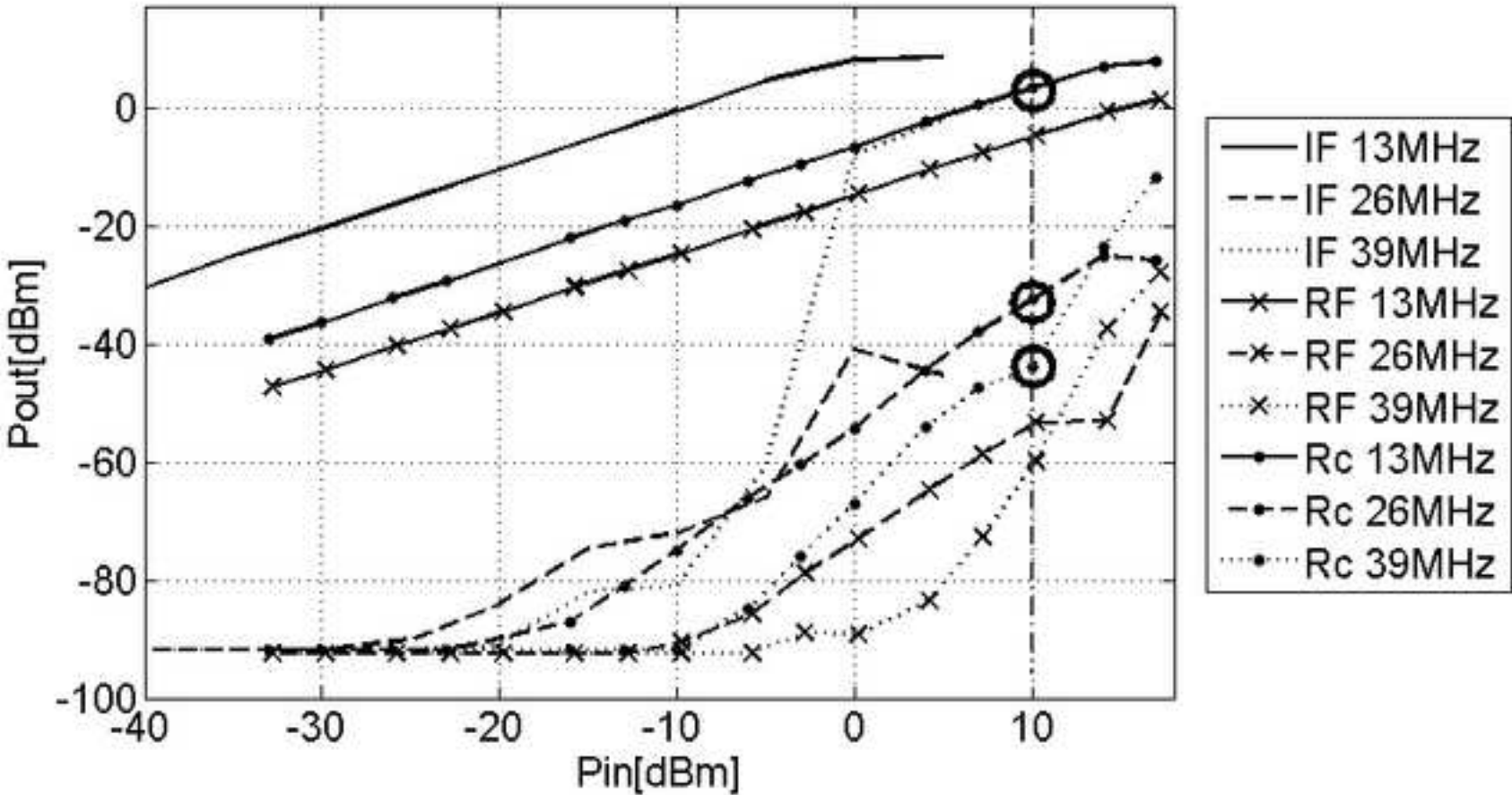


Table 1

		<i>Input Channels</i>							
		<i>1</i>	<i>2</i>	<i>3</i>	<i>4</i>	<i>5</i>	<i>6</i>	<i>7</i>	<i>8</i>
<i>Output Channels</i>	<i>1</i>	X	-80	-88	-86	-88	-87	-84	-87
	<i>2</i>	-86	X	-87	-83	-88	-88	-89	-87
	<i>3</i>	-87	-83	X	-81	-88	-90	-90	-87
	<i>4</i>	-88	-88	-82	X	-81	-87	-90	-88
	<i>5</i>	-89	-89	-89	-85	X	-80	-89	-88
	<i>6</i>	-89	-89	-90	-87	-80	X	-86	-88
	<i>7</i>	-86	-89	-89	-87	-86	-84	X	-83
	<i>8</i>	-88	-89	-90	-87	-88	-88	-87	X

Table 2

Measured Parameter	Measured Value	Expected Value
Amplitude Noise	0.0022% (10 Hz - 100kHz)	0.08 % (DC-100 kHz)
Phase Noise	0.0044° (10 Hz - 100kHz)	0.024 ° (DC-100 kHz)
Linearity	-50dBc (2 nd), -55dBc (3 rd)	< -75dBc
Harmonics Content	-80dBc (filtered output)	< -75dBc
Temperature Sensitivity	0.5 °/°C , 0.1 %/ °C	N/A
Coupling	from -80dB to -90dB	< -90 dB
Power Dissipation	1.7 W / ch (96 ch)	2 W / ch (96 ch)
Output power	+4dBm at 13MHz	> +3dBm at 13 MHz
Price	100\$ / channel (96 ch)	< 200\$/ channel (96 ch)